

RPN

Notice of Allowability	Application No.	Applicant(s)	
	10/771,564	JUENGLING ET AL.	
	Examiner	Art Unit	
	William C. Vesperman	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. This communication is responsive to 2/4/2002.
2. The allowed claim(s) is/are 1- 15.
3. The drawings filed on 04 February 2004 are accepted by the Examiner.
4. Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some* c) None of the:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
6. CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) hereto or 2) to Paper No./Mail Date _____.
 - (b) including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying Indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. Notice of References Cited (PTO-892)
2. Notice of Draftperson's Patent Drawing Review (PTO-948)
3. Information Disclosure Statements (PTO-1449 or PTO/SB/08),
Paper No./Mail Date 5/7/2004
4. Examiner's Comment Regarding Requirement for Deposit
of Biological Material
5. Notice of Informal Patent Application (PTO-152)
6. Interview Summary (PTO-413),
Paper No./Mail Date _____.
7. Examiner's Amendment/Comment
8. Examiner's Statement of Reasons for Allowance
9. Other _____.

DETAILED ACTION

1. This action is in response to applicant's filing of 2/4/2002.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with John Reed on June 17, 2004.

Please replace Claims 1, 14 and 15 with revised Claims 1, 14 and 15 as shown below.

1. A device comprising a memory cell, wherein said memory cell comprises:
 - a semiconductor substrate;
 - a switching device disposed over said semiconductor substrate;
 - a charge storage device in electrical communication with said switching device;
 - a plurality of topographic structures comprising:
 - at least one first topographic structure including conductive lead lines deposited over said semiconductor substrate and in electrical communication with said switching device, said at least one first topographic structure including a top surface; and
 - a plurality of second topographic structures with top surfaces thereon, said top surfaces of said second topographic structures generally coplanar with said top surfaces of said at least one first topographic structure;
 - at least one geometrically simple array comprising at least a portion of said

topographic structures such that:

a substantially continuous straight-edged periphery around said array is defined by said plurality of topographic structures; and no portion of said plurality of second topographic structures within said array extends laterally beyond said periphery;

a gridded valley disposed within said array and including an interconnected series of spaces between adjacent topographic structures, wherein:

a lateral distance defining a width of any one of said series of spaces is substantially equal to that of another of said series of spaces within said gridded valley;

the longest linear dimension of each of said series of spaces is no longer than the longest dimension of any of said second topographic structures; and

no intersection defined by a crossing between any two of said interconnected series of spaces includes uninterrupted linear dimensions; and

a planarization layer deposited over said substrate such that it is disposed at least within said gridded valley and laterally surrounds said plurality of topographic structures.

14. A memory cell comprising:

a substantially planar semiconductor substrate defining first and second orthogonal in-plane dimensions;

a switching device disposed over said semiconductor substrate;

a charge storage device in electrical communication with said switching device;

a plurality of first topographic structures comprising conductive lead lines deposited over said semiconductor substrate and in electrical communication with said switching device, said topographic structures including a top surface;

a plurality of second topographic structures with top surfaces thereon, said plurality of second topographic structures comprising the same material as said plurality of first topographic structures and defining first and second in-plane dimensions, and at

least one of said fill patterns overlaps with at least one adjacent fill pattern along at least one of said first and second in-plane dimensions, wherein at least a portion of said second topographic structures are T-shaped, said top surfaces of said second topographic structures generally co-planar with said top surfaces of said plurality of first topographic structures;

at least one geometrically simple array comprising at least a portion of said plurality of first and second topographic structures arranged over said semiconductor substrate such that:

a substantially continuous straight-edged periphery around said array is defined by said plurality of first topographic structures, second topographic structures or both; and
no portion of said plurality of second topographic structures within said array extends laterally beyond said periphery;

a gridded valley disposed within said array, said gridded valley comprising a first set of interconnected series of spaces that extend in said first orthogonal in-plane dimension, and a second set of said interconnected series of spaces that extend in said second orthogonal in-plane dimension such that:

said first and second set of interconnected series of spaces between adjacent ones of said first and second topographic structures define a width of any one of said interconnected series of spaces between 0.25 and 0.5 micron; the longest linear dimension of each of said interconnected series of spaces is no longer than the longest dimension of any of said second topographic structures; and
no intersection defined by a crossing between any two of said interconnected series of spaces includes uninterrupted linear dimensions; and

a TEOS planarization layer deposited over said substrate such that it is disposed at least within said gridded valley and laterally surrounds said plurality of first and second topographic structures.

15. A device comprising a memory cell, wherein said memory cell comprises:

a substrate with a plurality of peaks and valleys, where said peaks are defined by at least one topographic conductive line spaced apart from a plurality of topographic dummy patterns, and said valleys are defined by interpeak spaces that are formed between said peaks;

a switching device disposed over said semiconductor substrate;

a charge storage device in electrical communication with said switching device;

a repeating array defined by at least a portion of said plurality of peaks and valleys, wherein:

a substantially continuous straight-edged periphery around said array is defined by said topographic conductive line, dummy patterns or both; and

no portion of any of said plurality of said dummy patterns within said array extends laterally beyond said periphery of said array;

a grid disposed within said array, said grid defined by said interpeak spaces such that the longest linear dimension of each of said valleys is no longer than the longest lateral dimension of any of said dummy patterns, and no intersection defined by a crossing between any two of said interpeak spaces includes uninterrupted linear dimensions; and

a substantially planar layer of insulative material deposited over said valleys, said planar layer having a thickness selected to render a top surface of said substantially planar layer substantially co-planar with a top surface of said peaks.

Reasons For Allowance

3. Claims 1 – 15 are allowed.
4. The following is an examiner's statement of reasons for allowance.

Harvey (US 5,854,125) discloses (Figures 2d, 3a – 3c) a method of fabricating a semiconductor wafer, comprising: providing a generally planar semiconductor wafer

substrate such that the substrate is defined by substantially orthogonal first and second in-plane dimensions, defining a topographic layer of conductive lead line material such that said topographic layer projects onto the substrate to occupy at least a portion of the substantially orthogonal first and second in-plane dimensions; depositing at least one topographic layer of conductive lead line material on the substrate, depositing a plurality of topographic fill patterns adjacent either the topographic layer of conductive lead line material or another of the plurality of topographic fill patterns such that spaces defined there between possess substantially equal width as any other space and depositing a planarization layer over the substrate such that it is disposed at least within the grid and laterally surrounds the at least one topographic layer of conductive lead line material and the plurality of topographic fill patterns.

The prior art does not teach or fairly suggest, in combination with the other claimed limitations, a device where the arranging of a plurality of topographic fill patterns and at least one topographic layer of conductive lead line material creates a grid defined by a plurality of crossings of spaces containing no linear dimension longer than the longest dimension of any one of the plurality of topographic fill patterns; that no intersection defined by any of said plurality of crossings includes uninterrupted linear dimensions; and defining an array comprising of said plurality of topographic fill patterns and conductive lead line material such that a substantially continuous straight-edged periphery around said array is defined by said topographic fill patterns and conductive lead line material, and no portion of any of said topographic fill patterns overhangs a boundary of said array.

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Takizawa (US 6,504,254) teaches a semiconductor device with dummy wiring layers.

Chen et al. (US 6,178,853 B1) teaches a method of designing active patterns with a shifted dummy pattern.

Gabriel et al. (US 5,861,342) teaches a method of improving the planarity of spin on glass layers.

Findley et al. (US 5,763,955) teaches integrated filled layers for integrated circuits.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William C. Vesperman whose telephone number is 571-272-1701. The examiner can normally be reached on Mon. - Fri., 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl White, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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June 18, 2004

Tuan H. Nguyen

Tuan H. Nguyen
Primary Examiner